The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. A semiconductor inverter comprising:

a semiconductor substrate;

an insulator formed on said semiconductor substrate;

a semiconductor layer formed on said insulator;

a p-well formed in said semiconductor layer, said p-well being the output of said inverter;

a gate structure formed atop said p-well, said gate structure being the input of said inverter and being formed from a thin gate oxide layer underneath a conductive layer;

an n- base formed adjacent to a first edge of said gate structure;

a p+ structure formed within said n- base; and

a n+ structure adjacent a second edge of said gate structure.

2. The inverter of Claim 1 wherein said p-well extends through said semiconductor layer to said insulator.

3. The inverter of Claim 1 wherein said p+ structure and said n+ structure extend through said semiconductor layer to said insulator.

4. The inverter of Claim 1 wherein said semiconductor layer is less than 1500 angstroms thick.

5. The inverter of Claim 1 wherein said p- well is the output of said inverter.

6. A semiconductor inverter comprising

a semiconductor substrate;

an insulator formed on said semiconductor substrate;

a semiconductor layer formed on said insulator;

an n-well formed in said semiconductor layer, said n-well being the output of said inverter;

a gate structure formed atop said n-well, said gate structure being the input of said inverter and being formed from a thin gate oxide layer underneath a conductive layer;

an p- base formed adjacent to a first edge of said gate structure;

a n+ structure formed within said p- base; and

a p+ structure adjacent a second edge of said gate structure.

7. The inverter of Claim 6 wherein said n-well extends through said semiconductor layer to said insulator.

8. The inverter of Claim 6 wherein said p+ structure and said n+ structure extend through said semiconductor layer to said insulator.

9. The inverter of Claim 6 wherein said semiconductor layer is less than 1500 angstroms thick.

10. The inverter of Claim 6 wherein said n- well is the output of said inverter.

11. A NAND logic circuit having a first input and a second input comprising:

a semiconductor substrate;

an insulator formed on said semiconductor substrate;

a semiconductor layer formed on said insulator;

a p-well formed in said semiconductor layer;

a first gate structure formed atop said p-well, said first gate structure being the first input and being formed from a thin gate oxide layer underneath a conductive layer;

a second gate structure formed atop said p-well, said first gate structure being the second input and being formed from a thin gate oxide layer underneath a conductive layer;

a p+ structure formed adjacent to a first edge of said first gate structure and said second gate structure, said p+ structure being the output of said NAND logic circuit;

a n+ structure adjacent a second edge of said first gate structure and said second gate structure;

a first switch formed in said semiconductor layer, said first switch electrically connected to said first input;

a second switch formed in said semiconductor layer in series to said first switch and electrically connected to said second input, said second switch also electrically connected to said p+ structure.

12. The NAND gate of Claim 11 wherein said p-well extends through said semiconductor layer to said insulator.

13. The NAND gate of Claim 11 wherein said p+ structure and said n+ structure extend through said semiconductor layer to said insulator.

14. The NAND gate of Claim 11 wherein said semiconductor layer is less than 1500 angstroms thick.

15. A NAND logic circuit having a first input and a second input comprising:

a semiconductor substrate;

an insulator formed on said semiconductor substrate;

a semiconductor layer formed on said insulator;

a n-well formed in said semiconductor layer;

a first gate structure formed atop said n-well, said first gate structure being the first input and being formed from a thin gate oxide layer underneath a conductive layer;

a second gate structure formed atop said n-well, said first gate structure being the second input and being formed from a thin gate oxide layer underneath a conductive layer;

a n+ structure formed adjacent to a first edge of said first gate structure and said second gate structure, said n+ structure being the output of said NAND logic circuit;

a p+ structure adjacent a second edge of said first gate structure and said second gate structure;

a first switch formed in said semiconductor layer, said first switch electrically connected to said first input;

a second switch formed in said semiconductor layer in series to said first switch and electrically connected to said second input, said second switch also electrically connected to said n+ structure.

16. The NAND gate of Claim 15 wherein said n-well extends through said semiconductor layer to said insulator.

17. The NAND gate of Claim 15 wherein said p+ structure and said n+ structure extend through said semiconductor layer to said insulator.

18. The NAND gate of Claim 15 wherein said semiconductor layer is less than 1500 angstroms thick.

19. A NOR logic circuit having a first input and a second input comprising:

a semiconductor substrate;

an insulator formed on said semiconductor substrate;

a semiconductor layer formed on said insulator;

a p-well formed in said semiconductor layer;

a first gate structure formed atop said p-well, said first gate structure being the first input and being formed from a thin gate oxide layer underneath a conductive layer;

a second gate structure formed atop said p-well, said first gate structure being the second input and being formed from a thin gate oxide layer underneath a conductive layer;

an n- base formed adjacent to a first edge of said first gate structure and said second gate structure;

a p+ structure formed within said n- base;

a second p+ structure adjacent a second edge of said first gate structure and said second gate structure, said second p+ structure being the output of said NOR logic circuit;

a first switch formed in said semiconductor layer, said first switch electrically connected to said first input; and

a second switch formed in said semiconductor layer in series to said first switch and electrically connected to said second input, said second switch also electrically connected to said second p+ structure.

20. The NOR gate of Claim 19 wherein said p-well extends through said semiconductor layer to said insulator.

21. The NOR gate of Claim 19 wherein said p+ structure and said n+ structure extend through said semiconductor layer to said insulator.

22. The NOR gate of Claim 19 wherein said semiconductor layer is less than 1500 angstroms thick.

23. A NOR logic circuit having a first input and a second input comprising:

a semiconductor substrate;

an insulator formed on said semiconductor substrate;

a semiconductor layer formed on said insulator;

a n-well formed in said semiconductor layer, said n-well being the output of said NOR gate;

a first gate structure formed atop said n-well, said first gate structure being the first input and being formed from a thin gate oxide layer underneath a conductive layer;

a second gate structure formed atop said n-well, said first gate structure being the second input and being formed from a thin gate oxide layer underneath a conductive layer;

an p+ structure formed adjacent to a first edge of said first gate structure and said second gate structure;

a second p+ structure adjacent a second edge of said first gate structure and said second gate structure, said second p+ structure being the output of said NOR logic circuit;

a first switch formed in said semiconductor layer, said first switch electrically connected to said first input; and

a second switch formed in said semiconductor layer in series to said first switch and electrically connected to said second input, said second switch also electrically connected to said second p+ structure.

24. The NAND gate of Claim 23 wherein said n-well extends through said semiconductor layer to said insulator.

25. The NAND gate of Claim 23 wherein said p+ structure and said second p+ structure extend through said semiconductor layer to said insulator.

26. The NAND gate of Claim 23 wherein said semiconductor layer is less than 1500 angstroms thick.